WHAT IS CLAIMED IS:

Sub A6

1. A method for manufacturing a semiconductor device comprising the steps of:

forming a dummy gate electrode on a semiconductor substrate;

with the dummy gate electrode used as a mask, forming one pair of first impurity diffusion layers in those regions of the semiconductor substrate which are opposite to each other through the dummy gate electrode;

forming an insulating film on the semiconductor substrate in a way to bury the dummy gate electrode, while exposing an upper surface of the dummy gate electrode;

removing the dummy gate electrode and forming a first trench in the insulating film;

enlarging the width of the first trench and forming a second trench in the insulating film which is greater in width than the width of the first trench;

forming a gate insulating film along an inner surface of the second trench; and

forming a gate electrode in the second trench with the gate insulating film intervening therebetween.

2. The method according to claim 1, further comprising the steps of:

after forming the first impurity diffusion layers, forming a side wall insulating film on a side wall

surface of the dummy gate electrode; and

with the dummy gate electrode and the sidewall insulating film used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

3. The method according to claim 1, wherein the step of forming a second trench includes a step of performing an isotropic etching on the insulating film having the first trench formed therein.

4. The method according to claim 1, wherein the step of forming a gate insulating film includes a step of forming a gate insulating film in a manner to make the width of the second trench equal to, or greater than, that of the first trench.

5. The method according to claim 1, wherein the step of forming the gate insulating film includes a step of using an insulating material having a relative dielectric constant of above 5.

6. The method according to claim 1, wherein the step of forming a gate insulating film includes a step of using one selected from the group consisting of Ta_2O_5, silicon nitride, Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

7. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first insulating film on a semiconductor

substrate;

sequentially forming a first semiconductor film and a second insulating film on the first insulating film;

forming a resist pattern on the second insulating film;

with the resist pattern used as a mask, patterning the first semiconductor film and the second insulating film by an anisotropic etching to provide a stacked layer structure of the first semiconductor film and the second insulating film on the semiconductor substrate;

with the stacked layer structure used as a mask, ion-implanting an impurity in the semiconductor substrate to provide first impurity diffusion layers for a source and a drain;

forming a third insulating film over the semiconductor structure to bury the stacked layer structure;

etching back the third insulting film to expose an upper surface of the stacked layer structure;

with the third insulating film used as a mask, removing the stacked layer structure to form a trench in the third insulating film;

after forming the trench, enlarging the width of the trench by an isotropic etching;

after enlarging the width of the trench, depositing a fourth insulting film along an inner

surface of the trench; and

forming a conductive layer of a gate electrode on the fourth insulating film.

8. The method according to claim 7, further comprising the steps of:

after providing the first impurity diffusion layers, forming a sidewall insulating film on a sidewall of the stacked layer structure; and

with the sidewall insulating film and the stacked layer structure used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

9. The method according to claim 7, wherein the step of enlarging the width of the trench includes a step of using, as the isotropic etching, an etching treatment including HF or NH_4F.

10. The method according to claim 7, wherein the step of depositing a fourth insulating film includes a step of depositing a fourth insulating film by a chemical vapor deposition method or a sputtering method.

11. The method according to claim 7, wherein the step of depositing a fourth insulting film comprises a step of forming the fourth insulating film to make the width of the trench after forming the fourth insulating film equal to, or greater than, that of the first trench.

12. The method according to claim 7, wherein the step of depositing a fourth insulating film includes a step of using an insulating material having a dielectric constant of above 5.

13. The method according to claim 7, wherein the step of depositing a fourth insulating film includes a step of using one selected from the group consisting of Ta_2O_5, silicon nitride, Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

14. A semiconductor device comprising:

a semiconductor substrate;

a first impurity diffusion layer formed in the semiconductor substrate;

a second impurity diffusion layer formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer;

a first insulating layer formed on the first impurity diffusion layer;

a second insulating layer formed on the second impurity diffusion layer;

a trench formed over the semiconductor substrate in a manner to be defined between the first insulting layer and the second insulating layer;

a gate insulating film lined on a bottom surface and an inner sidewall surface of the trench; and

a gate electrode formed in the trench with the gate insulting film intervening therebetween, the gate

electrode being formed in an overlapped relation relative to the first impurity diffusion layer and the second impurity diffusion layer.

15. The semiconductor device according to claim 14, wherein the gate insulting film is formed of an insulting material having a dielectric constant of above 5.

16. The semiconductor device according to claim 14, wherein the gate insulating film contains one selected from the group consisting of Ta_2O_5, silicon nitride, Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide, and Ti oxide.

17. The semiconductor device according to claim 14, wherein the first impurity diffusion layer and the second impurity diffusion layer, each, comprise a third impurity diffusion layer including a portion formed beneath the gate insulating film formed on the inner sidewall surface of the trench and a fourth impurity diffusion layer including a portion formed beneath any of the first insulating layer and second insulating layer and having a deeper junction in the semiconductor substrate than the third impurity diffusion layer.

18. The semiconductor device according to claim 14, further comprising a metal silicide layer formed on the first impurity diffusion layer and the second impurity diffusion layer at those areas beneath the first insulating layer and the second insulating layer.